ABSTRACT

A delay-locked loop circuit generates a first clock signal. The delay-locked loop circuit includes a first delay element coupled in a feedback path of the delay-locked loop circuit to advance the first clock signal relative to a reference clock signal by a first time period. A second delay element is coupled to receive the first clock signal from the delay-locked loop circuit. The second delay element also outputs a second clock signal that is delayed relative to the first clock signal by the first time period. The delay-locked loop circuit may include a phase detector to identify phase differences between the first clock signal and the reference clock signal. A third delay element may be coupled between the delay-locked loop circuit and the second delay element.